REMARKS

1. Double Patenting rejection

The Examiner has provisionally rejected Claims 1, 3, 10 and 11 on the ground of obviousness-type double-patenting as being unpatentable over Claims 8-10, 16 and 18-19 of co-pending U.S. Patent Application 10/727,320 in view of Faucher. Claims 16-20 of U.S. Patent Application 10/727,320 have been canceled. Claims 8-10 of U.S. Patent Application 10/727,320 are directed to a processor in which power management is performed according to a global power consumption bound by communicating local power bounds to multiple device controllers, which may be memory controllers as recited in Claim 9, and/or in which the device controllers include usage evaluators that determine whether a usage of a device has fallen below a threshold.

None of the Claims of U.S. Patent Application 10/727,320 include both the input and output ports for reading and setting the state of the usage evaluators as recited in all of the independent claims of the present application. The Examiner indicated in the Final Office Action, that Faucher discloses such input and output ports and therefore makes Claims 1, 3, 10 and 11 of the present application obvious in light of U.S. Patent Application 10/727,320. However, as indicated in the above-described Telephonic Interview and as will be described in further detail below with respect to the rejection under 35

U.S.C. §102, applicants believe that Faucher does not disclose or suggest such input and output ports.

Therefore Applicants believe that the double-patenting rejection has been overcome.

2. Rejections under 35 U.S.C. §102

The Examiner has rejected Claims 1,3-11, 13 and 14 under 35 U.S.C. §102(b) as being anticipated by Faucher. Applicants respectfully disagree. Claim 1 (and similarly Claim 10) recites:

> "A device controller for coupling one or more controlled devices to one or more processors in a processing system, comprising:
> a command unit for sending commands to said one or more devices;
> at least one usage evaluator having an input coupled to an output of said command unit for evaluating a frequency of use of an associated controlled device;
> control logic coupled to said usage evaluator and further coupled to an input of said command unit for sending power management commands in response to said usage evaluator detecting that a usage level of said associated device has fallen below a threshold level, whereby said device controller power manages said controlled device without intervention by said one or more processors;
> **an output port coupled to said at least one usage evaluator for reading a state of said at least one usage evaluator, whereby a state of said at least one usage evaluator may be stored external to said device controller;** and
> **an input port coupled to said at least one usage evaluator for setting a state of said at least one usage evaluator, whereby said state of said at least one usage evaluator may be restored from information stored external to said device controller."**
>
> [**Bold text added for emphasis**]

The structure recited in Claim 1 enables reading from and writing to a usage evaluator through the recited input and output ports so that the state of the usage evaluator is preserved between process contexts, as recited in method Claim 15.

The structure described in Faucher does not enable preservation of such usage evaluator state information and Faucher does not describe any such action nor include an input and output port that enable such action with respect to the state of the usage evaluators.

In particular, in the Final Office Action, the Examiner indicated that the power management machine 66 of Faucher, includes an output port that sends data to programmable memory power system 24 that may be stored external to the memory controller. Faucher discloses two buses connected between programmable memory power system 24 and power management machine 66. The first bus is control buses 36, which carry signals that indicate which to which memory bank the data on the second bus, voltage programmable bus 46, applies. (Faucher, col. 4, lines 60-63.) The second bus, voltage programmable bus 46, digitally encodes the voltage to be applied to each memory bank and provides the digital representation of the voltage to programmable memory power system 24. The voltage is actually the result of a usage evaluation and not the state of the usage evaluator itself in the context of the present invention. (See the Specification at page 14, lines 25-32 in which the state of

the usage evaluators is described as being the state of the inter-arrival counts and/or statistics of usage evaluators 25A-D.)

In the Final Office Action, the Examiner also indicated that the power management machine 66 of Faucher includes an input port by which the state of the usage evaluator may be restored. However, Faucher does not restore the usage evaluator state via an input port, and if the usage evaluator state is taken as the above digital memory voltage representation that is "stored" in programmable memory power system 24, then there is no mechanism disclosed in Faucher to restore those values from programmable memory power system 24 to memory controller 20.

Further, during the Telephonic Interview described above, the Examiner indicated that he has subsequently determined that Faucher does not disclose such an input port.

In the Final Office Action, applicants note that the input port of Faucher cited by the Examiner was indicated as "an input port at which the usage evaluator receives data from outside of the memory controller from memory banks." However, Faucher discloses at col. 4, lines 41-47, that the information retrieved from the memory banks is merely configuration information, as typically supplied by a configuration bus (presence bus). The configuration information includes data regarding what banks are present, memory size, addressing, timing characteristics, which are simply the hard-wired characteristics of the particular

memory devices installed in the system and are provided for automatic system configuration. Therefore, the state retrieved by memory controller 20 from system memory 22 is not only not the state of usage evaluators, but is also not the same usage evaluator state asserted by the Examiner with respect to the output port element of the rejected Claims.

Therefore, for all of the reasons stated above, Applicants believe that the rejection under 35 U.S.C. §102(b) has been overcome.

3. Rejections under 35 U.S.C. §103

The Examiner has rejected Claims 15 and 18-20 under 35 U.S.C. §103(a) as being unpatentable over Faucher in view of Fleck, et al.(U.S. 6,128,641). Applicants respectfully disagree. For the reasons stated above, Faucher does not disclose the invention as recited in the independent Claims, and neither does the combination of Faucher and Fleck. Fleck discloses only an apparatus and methodology for saving state information upon a thread context switch and does concern usage evaluators, nor a device controller having input and output ports for saving the state of the usage evaluators.

Therefore, for all of the reasons stated above, Applicants believe that the rejection under 35 U.S.C. §103(a) has been overcome.

Therefore, for all of the reasons stated above, applicants believe that all of the rejections and objections have been overcome.

CONCLUSION

In conclusion, Applicants respectfully submit that this Response is fully responsive to all aspects of the objections and rejections tendered by the Examiner in the Final Office Action. Applicants respectfully submit that they have persuasively demonstrated that the above-identified Patent Application, including Claims 1,3-11, 13-15 and 17-20 are in condition for allowance, and such action is earnestly solicited.

No fees should be incurred by this Response, but if there are any fees incurred by this Response, please deduct them from IBM Deposit Account NO. 09-0447.

Respectfully Submitted,

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